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(54) ATM cell switching system.

(57) In a cell switching system having a plurality of input ports and a plurality of output ports in which cells of a fixed length packet input from said plurality of input ports are output from the desired output ports in accordance with address information added to each cell,
a cell distributing section is provided, corresponding to an input port, to separate input cells at a unit of cell to output them to thus selected output line, an output cell switching section is provided, corresponding to the output line of the cell distributing section, to detect address information added to the cell, and to output to the output line depending on a sequence inputted of cells towards the same output line without replacing such order, and a cell output control section is provided, corresponding to the output port, to perform a cell sequence aligning control. The cell switching section obtains the number of cells towards the same output line at the same time for each output line basis to transmit it together with an identifier indicating the corresponding cell switching section to the cell output control section, the cell output control section sequentially receives such information from the cell switching section, to extract the number of cells and the identifier from the received information which has fastest been input, and to send request signal for outputting one cell for the cell switching section indicated by the corresponding identifier, simultaneously the number of cells is subtracted by 1, wherein if a value of thus subtracted number reaches 0, the corresponding number of cells and the identifier information is discarded, and if a value of thus subtracted number of cells does not reach 0, the corresponding number is replaced by the subtracted value, thereby a cell output sequential aligning control is performed.

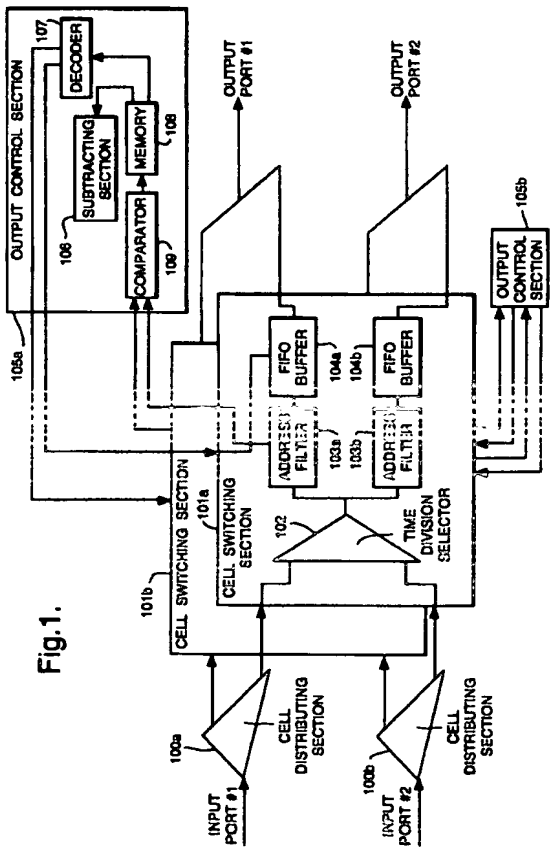

Fig.1.

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The present invention relates to an ATM (Asynchronous Transfer Mode) cell switching system, more especially one in which information such as voices, data, images are divided into each fixed length of cell and switched at a very high speed, and in particular relates to an ATM cell switching system capable of realizing a cell sequence control in the switching process using a simplified method.

Greatest concerns at the present time in this field are directed to the high speed cell switching system in which all the information such as voices, data, images are divided into cells each of which is a fixed length of packet, the information cellulated at a very high speed being transmitted and switched using a simplified protocol. For such cell switching device used in the high speed cell switching system, see the Articles, for example, Aramaki et al "Evaluation of Delay in the Cell Distribution Type High Speed ATM Switch" in the Proceedings of the 1991 Institute of Electronics Information, and Communication Engineers, Autumn Meeting, B-305. In such Articles there are described a cell distributing means provided corresponding to an input port, a plurality of cell switching means, and a cell sequential aligning means provided corresponding to an output port, where the cell distributing means selects one cell switching means from among said plurality of cell switching means, and outputs the cell given of the time stamp showing the input time to the cell switching means, said plurality of cell switching means perform the switching processes, the cell sequential aligning means outputs to the output port after aligning the cell output sequence using the time stamp given to the cell.

The conventional cell switching system is described as to its structure and operation using block diagrams in Figs. 4, 5, and 6 in the present application, assuming that two input lines are provided and a cell switching device is formed of two switch circuits.

Fig. 4 shows the cell switching device, wherein 400a, 400b depicts a cell distributing circuit, 401a, 401b switch circuits receiving outputs of the cell distributing circuits 400a, 400b as inputs respectively, and 402a, 402b cell sequence aligning circuits receiving outputs of the switch circuits 401a, 401b as inputs.

Fig. 5 shows the switch circuit, wherein 501 depicts a time division multiplex bus, 502a, 502b address filters connected to the time division multiplex bus 501, and 503a, 503b FIFO (First In First Out) buffers receiving outputs of the address filters 502a and 502b as inputs respectively.

Fig. 6 shows the cell sequence aligning means, wherein 601a, 601b depict cell sequence aligning memories, and 602 a time stamp minimum value detecting circuit performing outputting and inputting between the cell sequence aligning memories 601a, 601b in respect of information.

Figs. 4 to 6 designate examples of circuit operation. For the basic circuit operation shown by the examples in Figs. 4 and 5, the cell input from the input port is, at the cell distributing means 400a, 400b, given of the time stamp showing the input time, and is output to one switch circuit selected from a plurality of switch circuits. Thus the cell from the cell distributing means 400a, 400b is switched in accordance with address information given to the cell at the switch circuits 401a, 401b, and is output to the cell sequence aligning circuits 402a, 402b which is connected to the desired output ports. The cell sequence aligning circuits 402a, 402b output the cells to the output ports depending on the time stamp provided on the cell.

At that time, the switch circuit has a structure as shown in Fig. 5. The cell input from each input port of the switch circuit 500 is multiplexed in time division at the time division multiplex bus 501, and is input in a time divisional manner into the address filters 502a, 502b corresponding to each output port. The address filters 502a, 502b detect headers of the cells, subtract only the desirous cells, and output them to FIFO buffers 503a, 503b, which store and output the cells in a manner of "first in first out".

For operation of the cell sequence aligning circuit 600 in Fig. 6, the cells output from each switch circuit are stored in the cell sequence aligning memories 601a, 601b, provided at every switch circuit basis, which store and output the cells in way of first in first out. The time stamp minimum value detecting circuit 602 compares the time stamps given to the cells stored in the head part of the cell sequence aligning memories 601a, 601b, to detect the smallest time-stamp, and to transmit control signals so that the cell having the smallest time-stamp is to be output from the cell sequence aligning memories 601a, 601b.

As a disadvantage, the conventional cell exchange system must compare a plurality of time stamps ranging several bits, and further, on presence of a vacant cell sequence aligning memory, it must be confirmed that the cell having the smallest time stamp in the corresponding switch circuit does not exist. The present invention has been made for solving such problems. An aim of the invention is to provide an ATM cell exchange system capable of realizing a cell sequence control by a simplified method without using time stamp.

An ATM cell switching system according to the present invention, in a cell switching system having a plurality of input ports and a plurality of output ports in which cells of a fixed length packet input from said plurality of input ports are output from the desired output ports in accordance with address information added to such cells, is characterized by comprising,

a cell distributing section,

a cell switching section, and

a cell output control section, and further characterised in that;

the cell distributing section provided corresponding to

the input ports, has one input line connected to one of said plurality of input ports and a plurality of output lines, sequentially selects one output line from said plurality of output lines, separates cells input from the input ports into each cell unit, and outputs to the selected output line;

the cell switching sections arranged in the same number corresponding to output lines of the cell distributing section, have a plurality of input lines and a plurality of output lines, said plurality of input lines being connected respectively to the different output lines of the cell distributing section to detect address information added to each cell, the cell switching sections output cells towards the same output line keeping the sequence of input, and obtain the number of cells towards the same output lines at the same time for each output line basis, and transmit it together with an identifier indicating the corresponding cell switching section to the cell output control section;

the cell output control section provided corresponding to the output port, sequentially receives the information of the number of cells towards the output port at the same time transmitted from the cell switching section together with an identifier indicating the corresponding cell switching section, extracts the number of cells and the identifier from received information which has fastest be input, and sends out request signal to the cell switching section indicated by the corresponding identifier for outputting one cell, wherein the information of number of cells being subtracted by 1, if a value of thus subtracted number of cells reaches 0, the corresponding information of the number of cells and the identifier is discarded, and if a value of the subtracted number of cells does not reach 0, the corresponding number of cells is replaced by the subtracted value.

The cell switching section in the ATM cell switching system of the present invention, is characterized by comprising;

a time division selector accommodating a plurality of input lines of the cell switching section, selecting the cells input from each input line in time divisional manner to distribute into a plurality of output lines by the time division multiplexing;

an address filter provided corresponding to the output port, receiving the cells output from the time division selector, discriminating address information added to each cell, receiving and passing only the cells to be routed to the output ports corresponding to its own output ports, obtaining the number of cells received and passed through at the same time, and transmitting such information of the number of cells and the identifier indicating its own cell switching section to the cell output control section;

a first-in-first-out (FIFO) buffer provided corresponding to the address filter, storing the cells passed through such address filter at the arrived order, and outputting thus stored cells one by one at the arrived order to the output ports in accordamce with the instruction of the cell output control section.

The cell output control section in the ATM cell switching system of the present invention, is characterized by comprising;

a number of cells storage memory receiving a number of cells towards the same output line at the same time transmitted from the cell switching section and an identifier indicating the cell switching section, and storing such information at the received order;

a decoder recognizing the identifier of the information stored in the head part of the number of cells storage memory, and instructing a cell switching section corresponding to its identifier to output one cell to the output port;

a number of cells storage subtracting section reading the a value of number of cells stored in the head part of the number of cells storage memory, subtracting 1 from a value of such number of cells, in which if a value of thus subtracted number of cells reaches 0, the corresponding information of number of cells and the identifier is discarded, and if a value of thus subtracted number of cells does not reach 0, the corresponding number of cells is replaced by the subtracted value.

In this way, the ATM cell switching system of the present invention can perform sequence aligning control of the cells in accordance with the number of cells, towards the same output direction at the same time, calculated at every address filter basis of each cell switching section, without giving the time stamp indicating the input time of each cell.

Preferred features of the present invention will be described in further detail with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing one embodiment of an ATM cell switching system according to the present invention;

Fig. 2 is an illustrative view for illustrating operation of a cell distributing section and a cell switching section in Fig. 1;

Fig. 3 is an illustrative view for illustrating operation of an output control section in Fig. 1;

Fig. 4 is a block diagram showing one example of the conventional packet switching system;

Fig. 5 is an illustrative view illustrating the example of the switch circuit in Fig. 4; and

Fig. 6 is an illustrative view illustrating the example of the cell sequence aligning circuit in Fig. 4.

The present invention is described referring to the drawings. In the drawings hereinafter shown, it is assumed that each two of input ports and output ports and two sets of cell switching sections are provided respectively unless any particular explanation is otherwise provided.

Fig. 1 is a block diagram showing one embodiment of an asynchronous transfer mode (ATM) cell switching system according to the present invention,

which is a basic structure illustrating a principle of the invention.

In Fig. 1, 100a, 100b depict cell distributing sections, which are provided corresponding to the input ports and have functions in that a plurality of cells input from the input ports are separated into each cell unit, one input line and a plurality of output lines are provided therein, the input line is connected to the input port, one output line is sequentially selected from said plurality of output lines, the cells input from the input ports are output to the thus selected one output line. Numerals 101a, 101b depict cell switching sections, which are provided in a number equal to the number of output lines of the cell distributing sections 100a, 100b. The cell switching section has a plurality of input lines and a plurality of output lines, said plurality of input lines being connected to output lines of different cell distributing sections respectively, and detects address information of thus input cell, whereby the cells towards the same output line are output to the output line in the manner of the cell input sequence keeping such sequence order. The cell switching section functionally obtains the number of cells toward the same output line at the same time for each output line basis, and transmits such information to the cell output control section.

Numerals 105a, 105b depict output control sections, provided corresponding to the output ports, whose plurality of inputs are connected to different cell switching sections 101a, 101b respectively. The output control section is formed of a number of cells storage memory 108, a number of cells storage subtracting section 106, and a number of cells storage comparator 109. The number of cells storage comparator 109 receives the number of cells toward the same output line at the same time from the cell switching section together with an identifier designating such cell switching section, and if the number of cells is greater than zero, it is input into the number of cell storage memory 108. The number of cells storage subtracting section 106 extracts both the number of cells which has fastest been input into the number of cells storage memory 108, and an identifier corresponding to such number of cells, and transmits a request of cell output to the cell switching section designated by the identifier corresponding to such information of number of cells, the value of number of cells is subtracted by one, and if the subtracted value is less than zero, such information of number of cells and corresponding identifier is discarded from the number of cells storage memory 108, and if the subtracted value is more than zero, such number of cells is replaced with that subtracted value.

The cell distributing sections 100a, 100b may preferably have a function that a plurality of cells coming from the input ports are separated into a cell unit, each output direction of cells can sequentially be changed, and, in addition, the cell distributing sections corresponding to all the input ports are synchronously operated.

Each cell switching section 101a, 101b includes a time division selector 102, address filters 103a, 103b and FIFO buffers 104a, 104b. The time division selector 102, which is connected to each input line of the corresponding cell switching section, selects the cells input from each input line in time divisional manner, to multiplex in time division, and to distribute into a plurality of outputs. The address filters 103a, 103b, provided corresponding to each output port, whose each input is connected to the time division selector 102, receive the cells output from the time division selector 102 to discriminate address information of those cells which will be output to the corresponding output ports. Futhermore, the number of cells, toward the same output port, which has arrived at the time division selector 102 at the same time, are obtained and transmitted to the output control sections 105a, 105b. FIFO buffers 104a, 104b whose each input is connected to the address filters 103a, 103b, store the cells received by the address filters 103a, 103b, and output them to the output ports.

In the embodiment, the cell switching sections 101a, 101b are structured output buffer type cell switches having the cell buffers corresponding to each output port. However, if the same are structured cell switches performing the switching process and output of the cells keeping the sequence order, then both structures may preferably be available; namely, a common buffer type switch which the cell buffer corresponding to each output port is commonly used for all the output ports; and a cross point type switch having buffers at each cross point of input and output.

Each output control section 105a, 105b includes the number of cells storage comparator 109, the number of cells storage memory 108, a decoder 107, and the number of cells storage subtracting section 106. The input of the number of cells storage comparator 109 is connected to both of the number of cells indicating signal output from the address filters 103a, 103b of the cell switching sections 101a, 101b and the identifier signal output from the cell switching sections 101a, 101b, and selectively receives the numnber of cells indicating signal whose value is greater than zero in time division manner together with the identifier of the cell switching section which have processed those cells. The number of cells storage memory 108 is connected on its input with an output of the number of cells storage comparator 109, and stores and outputs the cell storage number output from the number of cells storage comparator 109 and the identifier of the cell switching section. The decoder 107 is connected on its input with an output of the number of cells storage memory 108, and in accordance with an identifier of the cell switching section output from the number of cells storage memory 108, a cell transmission request signal to the FIFO buffer

104a of the cell switching sections 101a, 101b is produced. The number of cells storage subtracting section 106 is connected on its input with the output of the number of cells storage memory 108, the value of the number of cells output from the number of cells storage memory 108 is subtracted by one, and if the value of the number of cells comes to zero, then the information of the number of cells which has fastest been input into the number of cells storage memory 108 from the number of cells storage comparator 109 and the identifier of the cell switching section is discarded, and in cases other than described above, the number of cells storage memory 108 is controlled in that the information of the number of cells which has fastest been input into the number of cells storage memory 108 from the number of cells storage comparator 109 is replaced by the value of the number of cells having been subtracted.

Figs. 2 and 3 show a cell switching section of Fig. 1, illustrating a basic operation of an output control section, Fig. 2 is an operation example relating to input ports to address filters, and Fig. 3 is an operation example of the output control section. For simplified explanation, it is assumed that the cells input from the input ports are all towards the output port #1.

The cells input from the input ports are separated into each cell unit by cell distributing sections 200a, 200b. Thus an input speed to each cell switching section 201a, 201b comes to the line speed of the input port / the number of cell switching sections. The cells input into the cell switching sections 201a, 201b are multiplexed by the time division selector 202, and are output to each address filter 203a, 203b. The address filters 203a and 203b, which are provided corresponding to the output ports, extracts only desired cell towards the corresponding output port to output it to the FIFO buffer. From among the cells input into the time division selector 202 at the same time during the gate being opened, the number of cells extracted by its own address filter and the identifier showing its own cell switching section both are output to the output control section.

In Fig. 3(A), in an output control section 307, the information of the identifier of the cell switching section which has fastest been input in the number of cells storage memory 304 in which the information of the number of cells and the identifier indicating a cell switching section is being stored in accordance with output of address filters 300a, 300b is extracted, and the cell output request signal is sent to FIFO buffers 301a or 301b of the corresponding cell switching section. At the same time of the above, the value of the number of cells is extracted from the number of cells storage memory 304, and after subtracting by one, the value before subtracting in respect of the number of cells storage memory 304 is renewed by the subtracted value. However, if the subtracted value is equal to zero as shown in Fig. 3(B), the value before subtraction together with the identifier of the cell switching section is discarded.

The buffers of the cell switching sections 302a, 302b perform storage and output of the cell in accordance with the rule of FIFO. The number of cells storage memory 304 stores both the identifier of the cell switching section and the cell number with reference to an inputted sequence ranging all the cell switching sections 302a, 302b, whereby the output controls of the cell switching sections 302a, 302b are performed. This provides an output from the buffers of the cell switching section while maintaining a cell sequence normal.

In Figs. 3(A) and 3(B), 300a, 300b depict address filters, 303 a number of cells storage comparator receiving outputs of the address filters 300a, 300b as inputs, 305 a decoder having an input of a cell switching section identifier 308 of the number of cells storage memory 304. The decoder 305 sends a cell output request to the buffers 301a, 301b of FIFO. Numeral 306 depicts a number of cells storage subtracting section receiving a stored number of cells 309 of the number of cells storage memory 304 as an input, and 307 an output control section for containing those described above.

As hereinbefore fully described, in an ATM cell switching system which processes the cell switching on the high speed transmission line using a plurality of cell switching sections, the present invention is capable of realizing a cell sequence control by a simplified method without using time stamp because the number of cells directing to the same output at the same time for each address filter basis of each cell switching section is calculated to perform the sequence aligning control of the cells in accordance with such calculated values.

The subject matter of the Abstract is incorporated into this description by reference by way of summary of the preferred features of the invention.

It will be understood that the present invention has been described above purely by way of example, and modifications of detail can be made within the scope of the invention.

Each feature disclosed in the description, and (where appropriate) the claims and drawings may be provided independently or in any appropriate combination.

Claims

1. An asynchronous transfer mode (ATM) cell switching system having a plurality of input ports and a plurality of output ports in which cells of a fixed length packet input from said plurality of input ports are output from the desired output ports in accordance with address information added to such cells,

characterized by comprising,
a cell distributing section,
a cell switching section, and
a cell output control section, and further characterised in that;
the cell distributing section provided corresponding to the input ports, has one input line connected to one of said plurality of input ports and a plurality of output lines, and is adapted sequentially to select one output line from said plurality of output lines, to separate cells input from the input ports into each cell unit, and to output to the selected one output line;
the cell switching sections are arranged in the same number as the output lines of the cell distributing section, and have a plurality of input lines and a plurality of output lines, said plurality of input lines being connected respectively to the different output lines of the cell distributing section to detect address information added to each cell, the cell switching sections being adapted to output cells towards the same output line keeping the sequence of input to obtain the number of cells towards the same output lines at the same time for each output line basis, and to transmit it together with an identifier indicating the corresponding cell switching section to the cell output control section;
the cell output control section is provided corresponding to the output port, for sequentially receiving theiinformation of the number of cells towards the output port at the same time transmitted from the cell switching section together with an identifier indicating the corresponding cell switching section, extracting the number of cells and the identifier from received information which has fastest been input, and sending out a request signal to the cell switching section indicated by the corresponding identifier for outputting one cell, wherein the information of the number of cells is subtracted by 1, and, if a value of thus subtracted number of cells reaches 0, the corresponding information of the number of cells and the identifier is discarded, and,if a value of the subtracted number of cells does not reach 0, the corresponding number of cells is replaced by the subtracted value.

2. An ATM cell switching system as claimed in claim 1, wherein the cell switching section is characterized by comprising:
a time division selector for accommodating a plurality of input lines of the cell switching section, and selecting the cells input from each input line in time divisional manner to distribute into a plurality of output lines by the time division multiplexing;
an address filter provided corresponding to the output port, for receiving the cells output from the time division selector, discriminating address information added to each cell, receiving and passing-only the cells to be routed to the output ports corresponding to its own output ports, obtaining the number of cells received and passed through at the same time, and transmitting such information of the number of cells and the identifier indicating its own cell switching section to the cell output control section; and
a first-in-first-out (FIFO) buffer provided corresponding to the address filter, for storing the cells passed through such address filter at the arrived order, and outputting thus stored cells one by one at the arrived order to the output ports in accordance with instruction of the cell output control section.

3. An ATM cell switching system as claimed in claim 1 or 2, wherein the cell output control section is characterized by comprising;
a number of cells storage memory for receiving a number of cells towards the same output line at the same time transmitted from the cell switching section and an identifier indicating the cell switching section, and storing such information at the received order;
a decoder for recognizing the identifier of the information stored in the head part of the number of cells storage memory, and instructing a cell switching section corresponding to its identifier to output one cell to the output port;
a number of cells storage subtracting section for reading a value of number of cells stored in the head part of the number of cells storage memory, and subtracting 1 from a value of such number of cells, in which if a value of thus subtracted number of cells reaches 0, the corresponding information of number of cells and the identifier is discarded, and if a value of thus subtracted number of cells does not reach 0, the corresponding number of cells is replaced by the subtracted value.

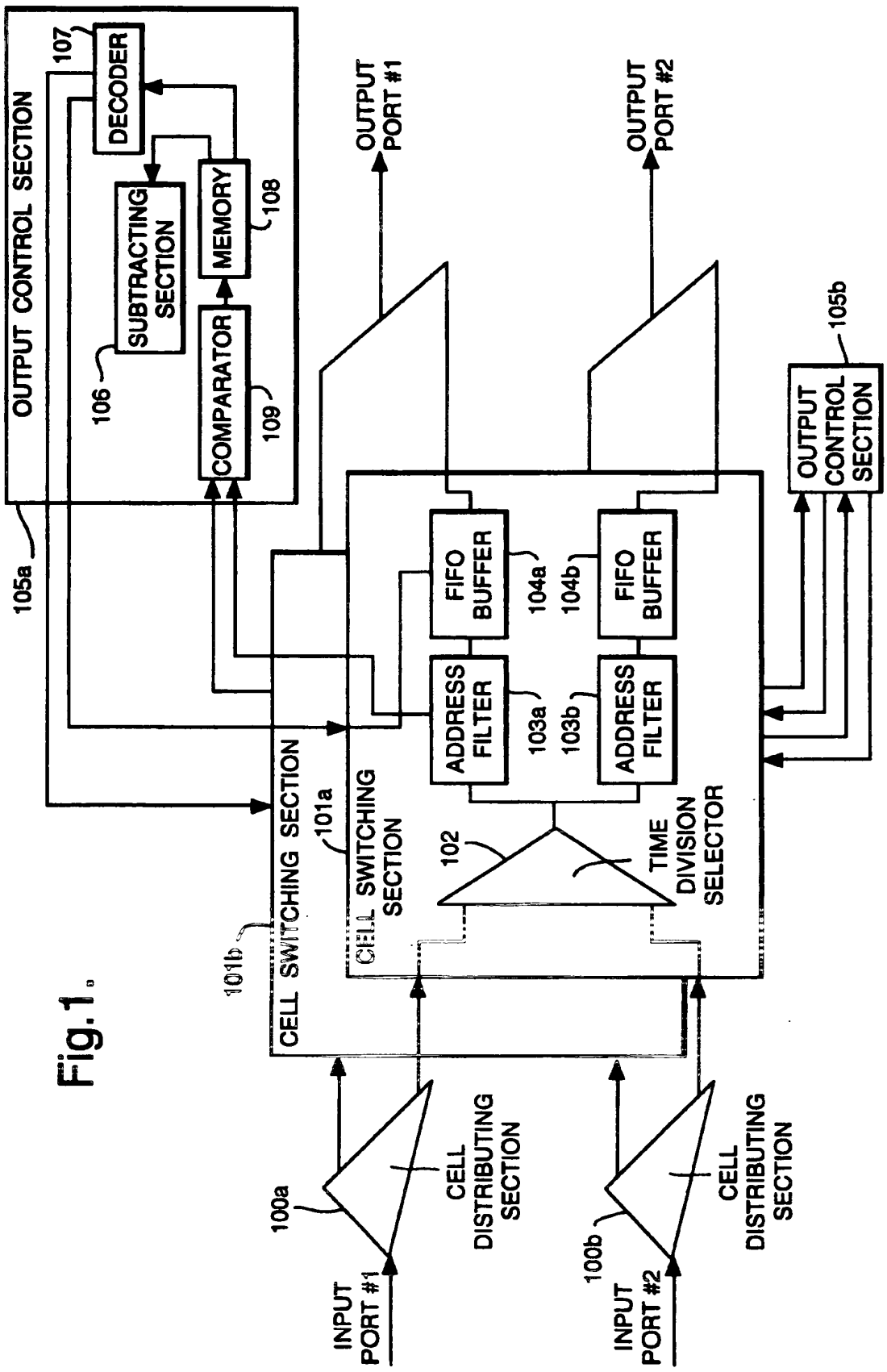
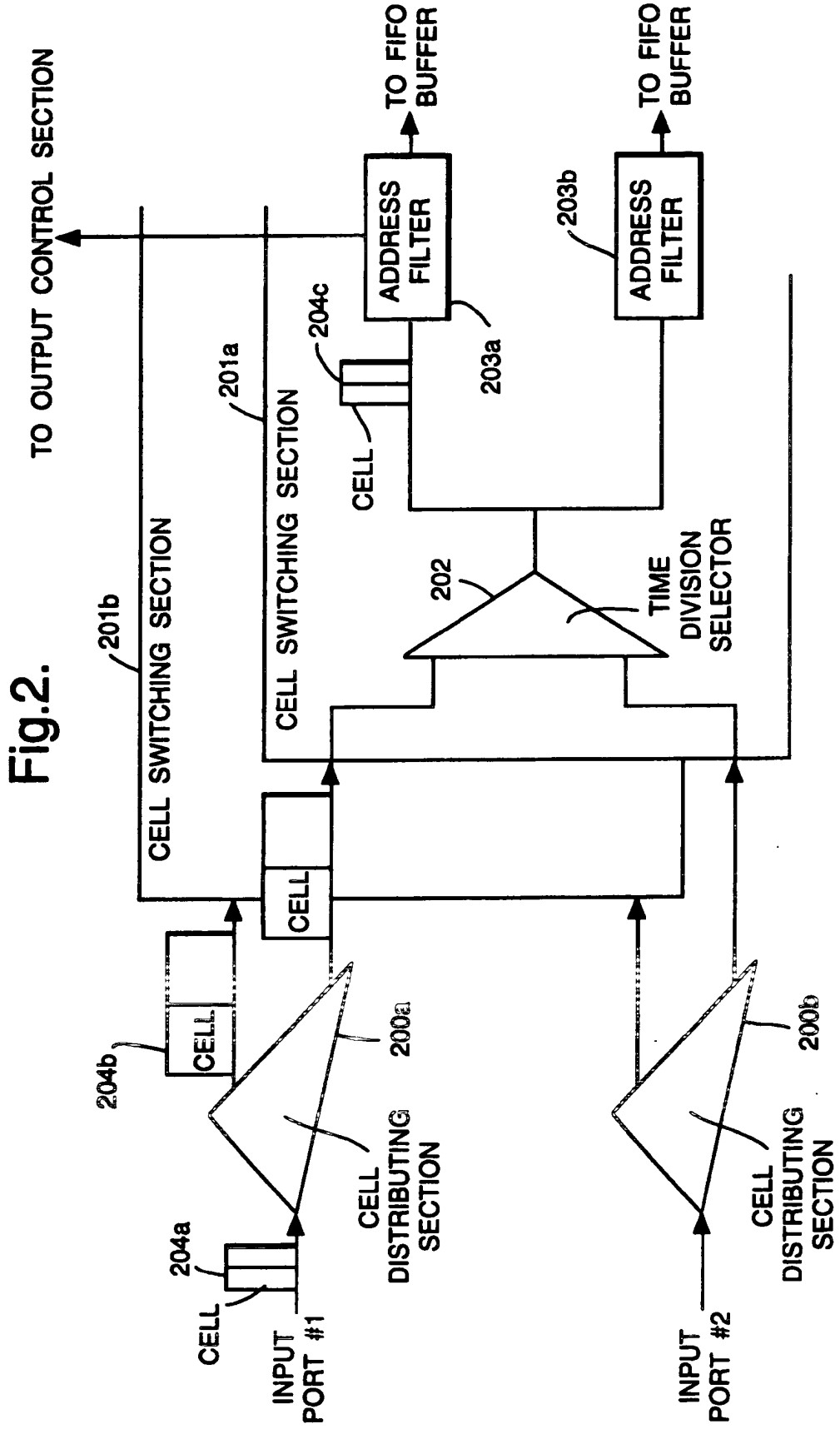

OUTPUT CONTROL SECTION
DECODER
107
SUBTRACTING SECTION
106
MEMORY
108
COMPARATOR
109
105a
OUTPUT PORT #1
OUTPUT PORT #2
105b
OUTPUT CONTROL SECTION
FIFO BUFFER
104a
104b
FIFO BUFFER
ADDRESS FILTER
103a
103b
ADDRESS FILTER
CELL SWITCHING SECTION
101a
101b
CELL SWITCHING SECTION
102
TIME DIVISION SELECTOR
100a
CELL DISTRIBUTING SECTION
100b
CELL DISTRIBUTING SECTION
INPUT PORT #1
INPUT PORT #2

Fig.1.

Fig.2.


TO OUTPUT CONTROL SECTION
TO FIFO BUFFER
TO FIFO BUFFER
ADDRESS FILTER
ADDRESS FILTER
203a
203b
204c
CELL
201a
CELL SWITCHING SECTION
201b
CELL SWITCHING SECTION
202
TIME DIVISION SELECTOR
CELL
CELL
204b
200a
200b
CELL DISTRIBUTING SECTION
CELL DISTRIBUTING SECTION
204a
CELL
INPUT PORT #1
INPUT PORT #2

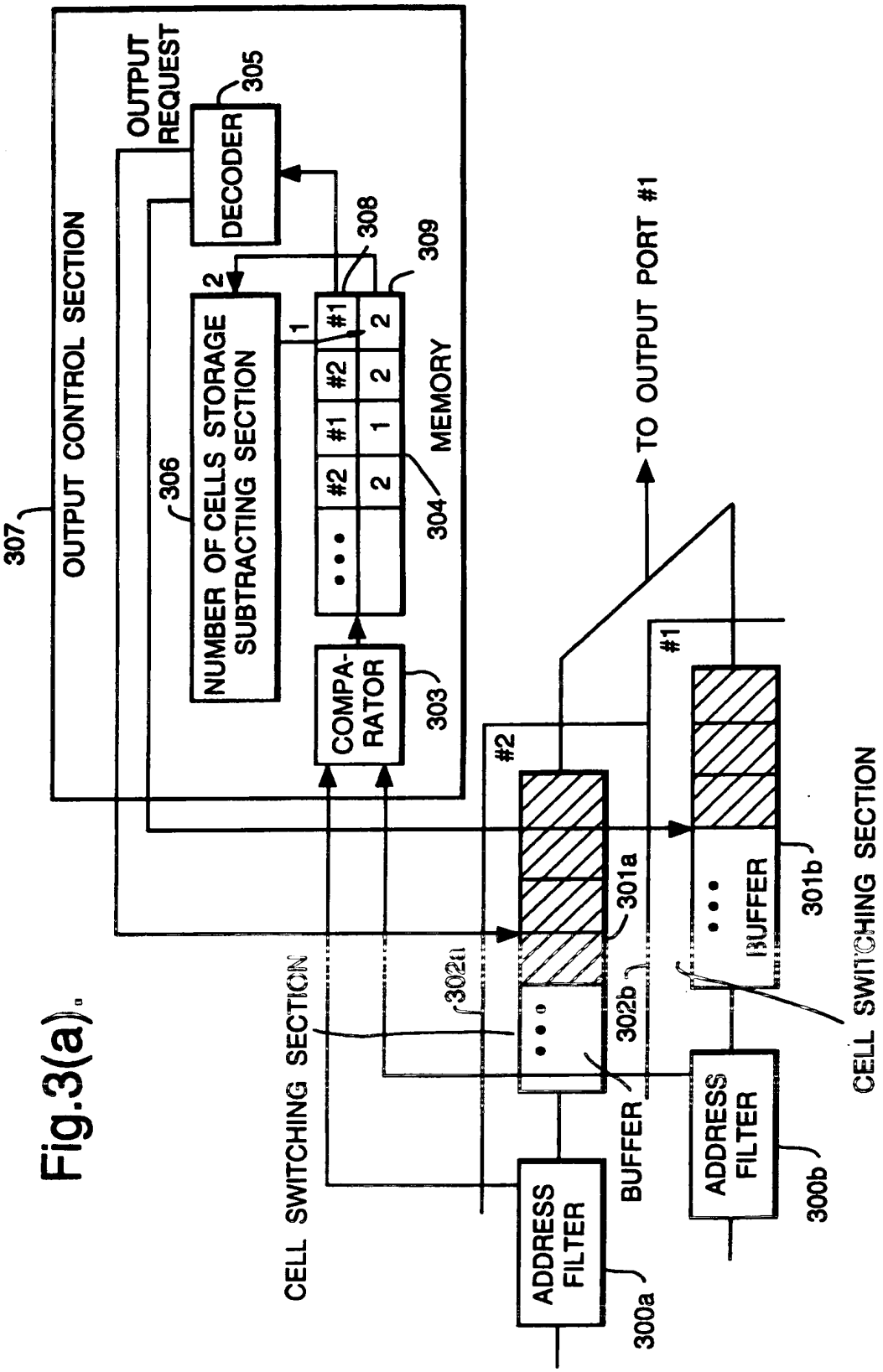

OUTPUT CONTROL SECTION
307
OUTPUT REQUEST
DECODER
305
NUMBER OF CELLS STORAGE SUBTRACTING SECTION
306
COMPA-RATOR
303
MEMORY
304
308
309
#1
#2
TO OUTPUT PORT #1
CELL SWITCHING SECTION
302a
302b
BUFFER
301a
301b
ADDRESS FILTER
300a
300b
CELL SWITCHING SECTION

Fig.3(a).

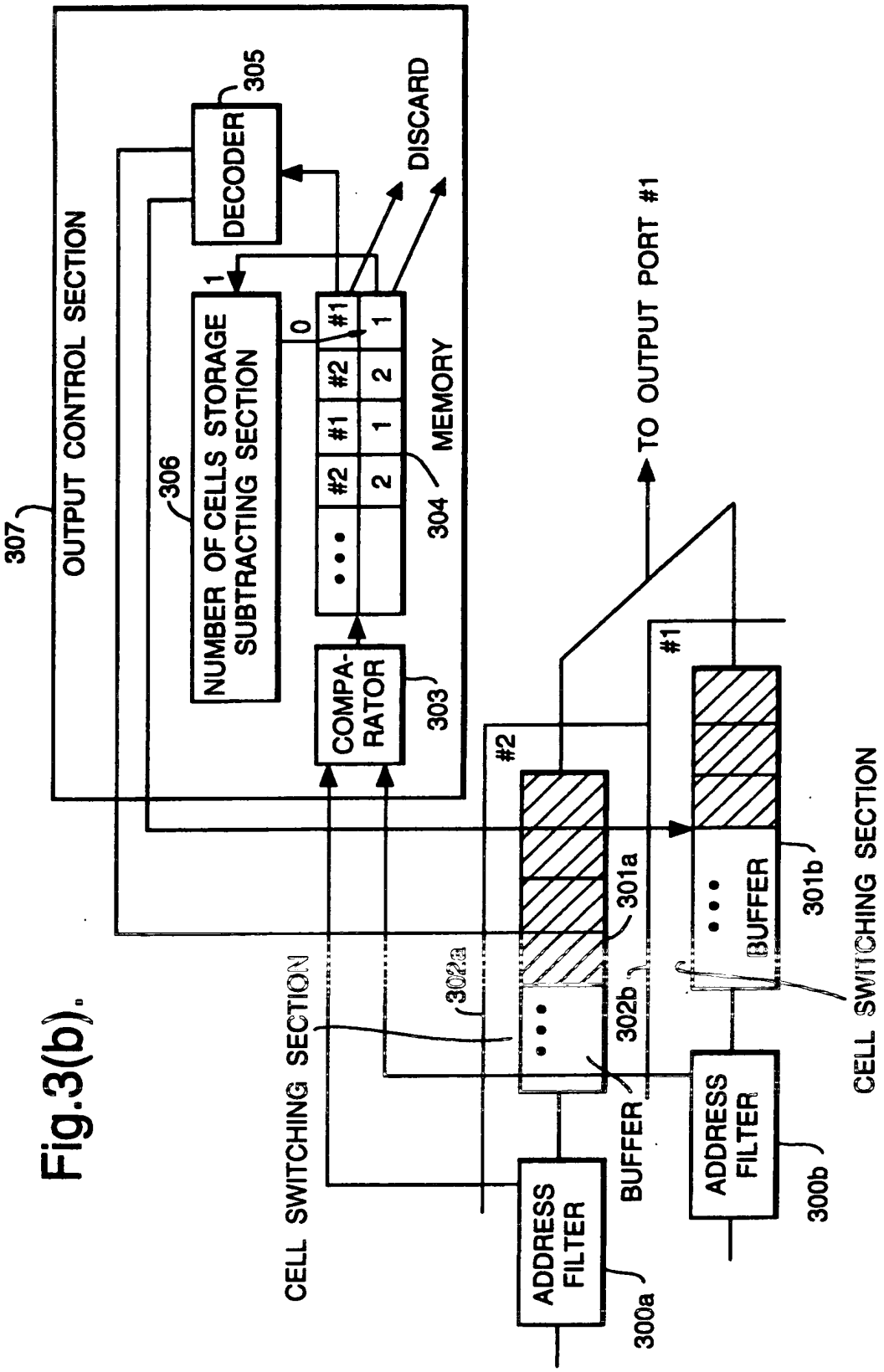

307
OUTPUT CONTROL SECTION
306
NUMBER OF CELLS STORAGE SUBTRACTING SECTION
DECODER
305
DISCARD
MEMORY
304
COMPA-RATOR
303
TO OUTPUT PORT #1
CELL SWITCHING SECTION
302a
302b
BUFFER
301a
301b
ADDRESS FILTER
300a
300b
#1
#2

Fig.3(b).

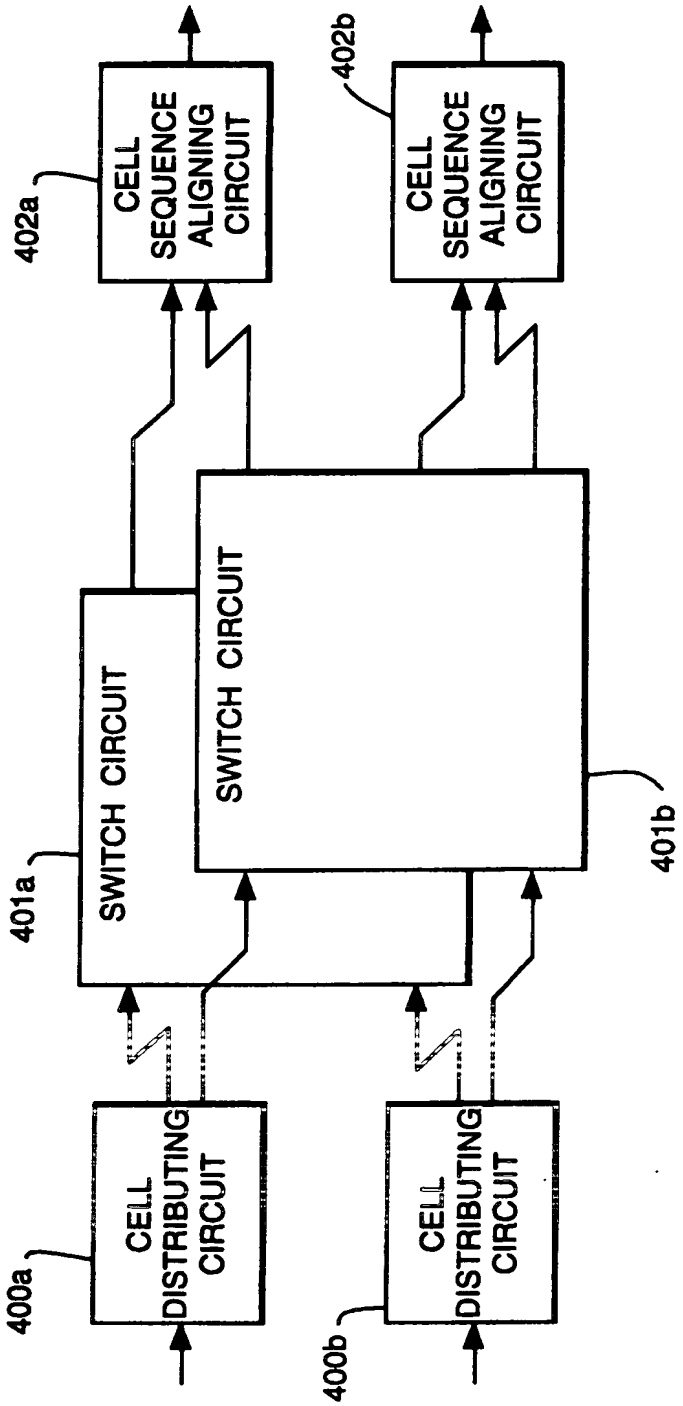


Fig.4.
(PRIOR ART)

Fig.5.
(PRIOR ART)

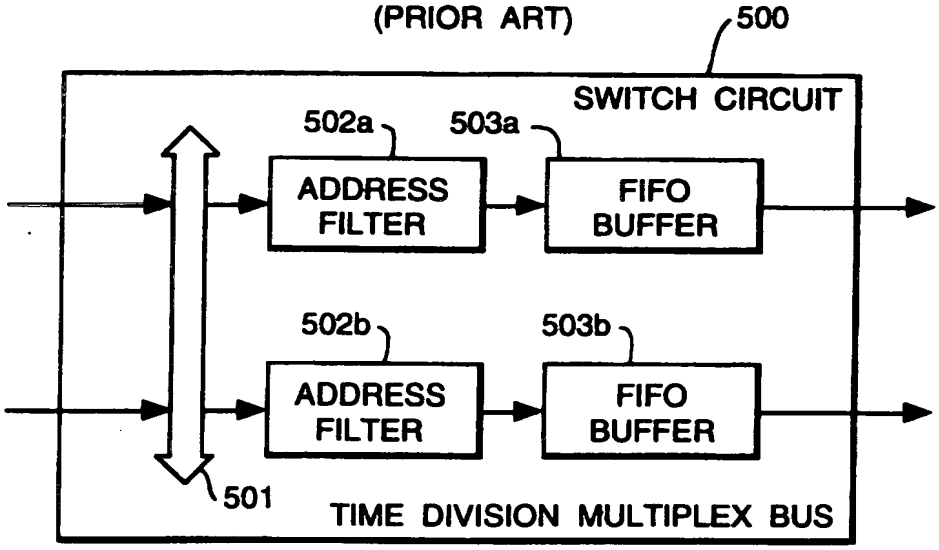


Fig.6.
(PRIOR ART)